IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellants: Marc Duranton et al.
Serial No.: 10/522,463
Filed: January 26, 2005
For: DATA PROCESSING CIRCUIT

Group Art Unit: 2193
Examiner: Malzahn, David H.
Confirmation No.: 3481

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF UNDER 37 C.F.R. § 41.37(a)

This is an appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner dated September 3, 2008, which finally rejected claims 1-3 and 5-8 in the above-identified application. The Office date of receipt of Appellants' Notice of Appeal was December 19, 2008. This Appeal Brief is hereby submitted pursuant to 37 C.F.R. § 41.37(a).

CERTIFICATE OF MAILING UNDER 37 C.F.R. 1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

Date:_____ Signed:_____

Typed Name: Mark A. Wilson

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST 4

II. RELATED APPEALS AND INTERFERENCES 4

III. STATUS OF CLAIMS 4

IV. STATUS OF AMENDMENTS 4

V. SUMMARY OF CLAIMED SUBJECT MATTER 4

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL 5

VII. ARGUMENT 5

A. Claim 1 is patentable over Dutta because Dutta does not disclose multiple separate functional units to perform n-taps polyphase filtering and m-taps polyphase filtering 6

B. The rejection of claim 2 is improper because the Examiner does not provide any substantive analysis of the specific limitations of the claim 8

C. The rejection of claim 3 is improper because the Examiner does not provide any substantive analysis of the specific limitations of the claim 8

D. The rejection of claim 5 is improper because the Examiner does not provide any substantive analysis of the specific limitations of the claim 9

E. The rejection of claim 6 is improper because the Examiner does not provide any substantive analysis of the specific limitations of the claim 9

F. The rejection of claim 7 is improper because the Examiner does not provide any substantive analysis of the specific limitations of the claim 9

G. The rejection of claim 8 is improper because the Examiner does not provide any substantive analysis of the specific limitations of the claim 9

VIII. CONCLUSION 11

IX. CLAIMS APPENDIX....12
X. EVIDENCE APPENDIX....14
XI. RELATED PROCEEDINGS APPENDIX....15

I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the full interest in the invention, NXP B.V., of Eindhoven, Netherlands.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellants' knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision in the instant appeal.

III. STATUS OF CLAIMS

Claim 1-3 and 5-8 are pending in the present application.

Claim 4 is canceled.

No claims are withdrawn.

No claims are objected to.

Claims 1-3 and 5-8 were finally rejected in the Office Action mailed September 3, 2008 as follows:

> Claims 1-3 and 5-8 stand rejected under 35 U.S.C. 102(e) as being anticipated by Dutta et al. (U.S. Pat. No. 6,963,890, hereinafter Dutta).

Claims 1-3 and 5-8 are the subject of this appeal. A copy of claims 1-3 and 5-8 is set forth in the Claims Appendix.

IV. STATUS OF AMENDMENTS

There were no proposed amendments submitted subsequent to the Final Office Action mailed September 3, 2008.

V. SUMMARY OF CLAIMED SUBJECT MATTER

This section of this Appeal Brief is set forth to comply with the requirements of 37 C.F.R. § 41.37(c)(1)(v) and is not intended to limit the scope of the claims in any way. Examples of implementations of the limitations of independent claim 1 are described below.

The language of claim 1 relates to a data processing system for performing polyphase filtering with a memory device to store data and coefficients. Page 1, lines 2-5, Fig. 3, data, coef, and results. The system is created from at least two functional units that are able to perform all types of polyphase filtering, including n-taps polyphase filtering and m-taps polyphase filtering, where m and n are integers greater than or equal to two. Page 1, lines 2-5. The functional units are able to receive data and coefficients from the memory device and to calculate results from the data and coefficients and supply them back to the memory device. Page 2, lines 25-28, Fig. 3, data, coef, and results. A crossbar is used to transfer data, coefficients and results between the memory device and any functional unit or any combination of functional units. Page 3, lines 25-27, Fig. 3, R-XBAR, W-XBAR.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claim 1 is patentable over Dutta under 35 U.S.C. 102(e).

B. Whether claim 2 is patentable over Dutta under 35 U.S.C. 102(e).

C. Whether claim 3 is patentable over Dutta under 35 U.S.C. 102(e).

D. Whether claim 5 is patentable over Dutta under 35 U.S.C. 102(e).

E. Whether claim 6 is patentable over Dutta under 35 U.S.C. 102(e).

F. Whether claim 7 is patentable over Dutta under 35 U.S.C. 102(e).

G. Whether claim 8 is patentable over Dutta under 35 U.S.C. 102(e).

VII. ARGUMENT

For the purposes of this appeal, claim 1 is argued separately for purposes of the question of patentability over Dutta under 35 U.S.C. 102(e). Claim 2 is argued separately for purposes of the question of patentability over Dutta under 35 U.S.C. 102(e). Claim 3 is argued separately for purposes of the question of patentability over Dutta under 35 U.S.C. 102(e). Claim 5 is argued separately for purposes of the question of patentability over Dutta under 35 U.S.C. 102(e). Claim 6 is argued separately for purposes of the question of patentability over Dutta under 35 U.S.C. 102(e). Claim 7 is argued separately for purposes of the question of patentability over Dutta under 35 U.S.C. 102(e). Claim 8

is argued separately for purposes of the question of patentability over Dutta under 35 U.S.C. 102(e).

A. Claim 1 is patentable over Dutta because Dutta does not disclose multiple separate functional units to perform n-taps polyphase filtering and m-taps polyphase filtering.

Appellants respectfully submit that claim 1 is patentable over Dutta because Dutta does not disclose all the limitations of the claim. Claim 1 recites:

> A data processing circuit comprising:
> a memory device to store data and coefficients;
> at least a first functional unit to perform a n-taps polyphase filtering and a second functional unit to perform a m-taps polyphase filtering, m and n being integers greater than or equal to two, wherein the functional units are able to receive in parallel data and coefficients coming from the memory device, and to calculate results from said data and coefficients and supply these results back to the memory device; and
> a crossbar to perform a transfer of the data, coefficients, and results between the memory device and any functional unit or any combination of functional units.

(Emphasis added.)

In contrast, Dutta does not disclose all of the limitations recited in claim 1 because Dutta does not disclose multiple separate functional units to perform n-taps polyphase filtering and m-taps polyphase filtering, as recited in the claim. Dutta merely describes a single functional unit within a digital filter architecture that can be readily reconfigured to operate in any of a plurality of filtering modes. Dutta, col. 4, lines 12-15. In particular, Dutta describes a hardware reconfigurable digital filter having selectable filtering modes. Dutta, col. 4, lines 18-21. The digital filter includes mode selection circuitry, logic circuitry, and computational circuitry. Dutta, col. 4, lines 21-23. The mode selection circuitry switches the digital filter between different multiple filtering modes depending on the particular application. Dutta, col. 4, lines 40-42. To illustrate this mode switching performance, Dutta provides two separate examples.

In one example, Dutta describes switching from a first filtering mode involving a high precision type of filtering to a second filtering mode involving a more common type of filtering operation. Dutta, col. 4, lines 42-48. In this example, the mode selection circuitry commands the orientation of the multiplication logic and addition circuits to

reconfigure the digital filter for the two modes. Dutta, col.4, lines 40-51. In other words, the mode selection circuitry controls how the hardware logic and circuitry within the digital filter is reconfigured, or physically changed, in order to switch from one filter mode to another.

In the other example, Dutta describes switching from one type of the more common filtering mode to another type of the more-common filtering mode. Dutta, col. 4, lines 64-66. Dutta states that the more common types of filtering modes include m-tap finite impulse response (FIR) and n-tap FIR filtering. Dutta, col. 4, line 66, through col. 5, line 2. In this example, the mode selection circuitry reconfigures the filter by controlling the orientation and communication of data between registers in the respective cells of the logic circuitry without changing the orientation of the multiplication logic and addition circuits in the computational circuitry. Dutta, col. 5, lines 3-15. In other words, the hardware configuration of the logic and circuitry within the digital filter is not changed, but the data stored in the registers is changed.

While the hardware-reconfigurable digital filter disclosed by Dutta can be reconfigured to perform different types of digital filtering modes, the hardware-reconfigurable digital filter can only perform one mode of digital filtering at a time and the number and types of filtering modes is determined by the configuration of the hardware. In other words, the types of filtering modes are hard wired into the circuit, and only those modes can be configured. In order to perform two modes of digital filtering, the same digital filter is reconfigured to switch from one digital filtering mode to another digital filtering mode. Hence, Dutta merely describes a single digital filter, even though the same digital filter can be reconfigured to perform different types of digital filtering modes. Therefore, Dutta does not disclose first and second functional units to perform filtering because Dutta merely describes a single digital filter.

One difference between an implementation that uses two separate function units to perform filtering, instead of a single hardware-reconfigurable digital filter, is that multiple filtering operations may be performed at the same time using separate functional units. In contrast, a single hardware-reconfigurable digital filter may be able to perform different types of filtering modes, but cannot perform the filtering modes at the same time or on separate data. For example, Dutta explains that the output from the first filtering

mode must be reloaded as input for a second filtering mode, presumably after the hardware of the digital filter is reconfigured. Dutta, col. 6, lines 30-33. Thus, a two pass filtering operation takes data from the output of one mode of filtering and reloads the output as input for the second mode of filtering because the reconfigurable hardware digital filter disclosed by Dutta is only a single functional unit that can only perform one mode of filtering at a time.

For the reasons presented above, Dutta does not disclose all of the limitations of the claim because Dutta does not disclose multiple separate functional units to perform n-taps polyphase filtering and m-taps polyphase filtering, as recited in the claim. Accordingly, Appellants respectively assert claim 1 is patentable over Dutta because Dutta does not disclose all the limitations of the claim.

Claims 2-3 and 5-8 depend from and incorporate all of the limitations of the corresponding independent claim 1, which is patentable over the cited reference. Therefore, dependent claims 2-3 and 5-8 are also patentable over the cited reference based on an allowable base claim. Additionally, each of claims 2-3 and 5-8 may be allowable for further reasons. Accordingly, Appellants request that the rejections of claims 1-3 and 5-8 under 35 U.S.C. 102(e) be withdrawn.

B. The rejection of claim 2 is improper because the Examiner does not provide any substantive analysis of the specific limitations of the claim.

The Examiner does not provide any substantive analysis based on the asserted grounds for rejection for dependent claim 2. In particular, the Examiner does not provide any analysis to support an assertion of anticipation under 35 U.S.C. 102 or to establish *prima facie* obviousness under 35 U.S.C. 103. Therefore, the Examiner does not establish a proper rejection for claim 2 under either 35 U.S.C. 102 or 103.

C. The rejection of claim 3 is improper because the Examiner does not provide any substantive analysis of the specific limitations of the claim.

The Examiner does not provide any substantive analysis based on the asserted grounds for rejection for dependent claim 3. In particular, the Examiner does not provide any analysis to support an assertion of anticipation under 35 U.S.C. 102 or to establish

prima facie obviousness under 35 U.S.C. 103. Therefore, the Examiner does not establish a proper rejection for claim 3 under either 35 U.S.C. 102 or 103.

D. The rejection of claim 5 is improper because the Examiner does not provide any substantive analysis of the specific limitations of the claim.

The Examiner does not provide any substantive analysis based on the asserted grounds for rejection for dependent claim 5. In particular, the Examiner does not provide any analysis to support an assertion of anticipation under 35 U.S.C. 102 or establish *prima facie* obviousness under 35 U.S.C. 103. Therefore, the Examiner does not establish a proper rejection for claim 5 under either 35 U.S.C. 102 or 103.

E. The rejection of claim 6 is improper because the Examiner does not provide any substantive analysis of the specific limitations of the claim.

The Examiner does not provide any substantive analysis based on the asserted grounds for rejection for dependent claim 6. In particular, the Examiner does not provide any analysis to support an assertion of anticipation under 35 U.S.C. 102 or establish *prima facie* obviousness under 35 U.S. C. 103. Therefore, the Examiner does not establish a proper rejection for claim 6 under either 35 U.S.C. 102 or 103.

F. The rejection of claim 7 is improper because the Examiner does not provide any substantive analysis of the specific limitations of the claim.

The Examiner does not provide any substantive analysis based on the asserted grounds for rejection for dependent claim 7. In particular, the Examiner does not provide any analysis to support an assertion of anticipation under 35 U.S.C. 102 or establish *prima facie* obviousness under 35 U.S.C. 103. Therefore, the Examiner does not establish a proper rejection for claim 7 under either 35 U.S.C. 102 or 103.

G. The rejection of claim 8 is improper because the Examiner does not provide any substantive analysis of the specific limitations of the claim.

The Examiner does not provide any substantive analysis based on the asserted grounds for rejection for dependent claim 8. In particular, the Examiner does not provide

any analysis to support an assertion of anticipation under 35 U.S.C. 102 or establish *prima facie* obviousness under 35 U.S.C. 103. Therefore, the Examiner does not establish a proper rejection for claim 8 under either 35 U.S.C. 102 or 103.

VIII. CONCLUSION

For the reasons stated above, claims 1-3 and 5-8 are patentable over the cited reference. Thus, the rejections of claims 1-3 and 5-8 should be withdrawn. Appellants respectfully request that the Board reverse the rejections of claims 1-3 and 5-8 under 35 U.S.C. 102(e) and, since there are no remaining grounds of rejection to be overcome, direct the Examiner to enter a Notice of Allowance for claims 1-3 and 5-8.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3444** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-3444** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

/mark a. wilson/

Date: February 19, 2009

Mark A. Wilson
Reg. No. 43,994

Wilson & Ham
PMB: 348
2530 Berryessa Road
San Jose, CA 95132
Phone: (925) 249-1300
Fax: (925) 249-0111

IX. CLAIMS APPENDIX

1. A data processing circuit comprising:

a memory device to store data and coefficients;

at least a first functional unit to perform a n-taps polyphase filtering and a second functional unit to perform a m-taps polyphase filtering, m and n being integers greater than or equal to two, wherein the functional units are able to receive in parallel data and coefficients coming from the memory device, and to calculate results from said data and coefficients and supply these results back to the memory device; and

a crossbar to perform a transfer of the data, coefficients, and results between the memory device and any functional unit or any combination of functional units.

2. A data processing circuit as claimed in claim 1, wherein at least one functional unit is able to function according to a direct mode and a transposed mode, the circuit comprising control means for controlling the functioning mode of said functional unit.

3. A data processing circuit as claimed in claim 1, wherein at least one functional unit is also able to perform a multiplication-accumulation using two data items coming from the memory device.

4. (canceled)

5. An image processing system comprising a processing circuit as claimed in claim 1.

6. A receiver decoder device for television comprising at least one image processing system as claimed in claim 5.

7. A device comprising at least one screen intended to display images and an image processing system as claimed in claim 5.

8. A communication network comprising at least one transmitter able to send signals representing at least one image, a transmission network, a receiver able to receive said signals and an image processing system as claimed in claim 5.

X. EVIDENCE APPENDIX

There is no evidence submitted with this Appeal Brief.

XI. RELATED PROCEEDINGS APPENDIX

To the best of Appellants' knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision in the instant appeal.